ABSTRACT OF THE DISCLOSURE

A method for testing a semiconductor memory device includes forcing the device into a logic state configuration that does not occur during normal operation of the device. The method may also include holding the logic state configuration for a user-variable length of time. In an embodiment, the device testing method includes flowing a direct current through a first input node of a bi-stable latch. This node may be electrically arranged between a node coupled to a voltage source and a node coupled to a circuit ground potential. An embodiment of a memory device may include testmode circuitry adapted to maintain a pair of bitlines at logic states that are not maintained during ordinary operation of the device. A system for testing a semiconductor memory device may include testmode circuitry adapted to force a pair of bitlines to the same logic state for a user-determined length of time.